ABSTRACT

With the advancement of the integrated circuit (IC) industry, there is a growing demand for battery-powered and low-power devices for portable applications in consumer electronics, medical science, communication, and automatic vehicles, *etc*. In mixed-signal circuits, analog circuits are about 20% in portion but consume 80% of the design time and effort, and have higher power, process variations and interference, whereas digital circuits are power efficient, robust, and require less design effort; thus, less time-to-market, has less process, voltage and temperature (PVT) variations and scalable. A methodology for designing analog/mixed signal circuits employing digital-in-concept circuits has been proposed in the present work. A flash ADC has been chosen to demonstrate this digital-in-concept circuit design methodology for SoC applications such as autonomous navigation, collision avoidance, distance measuring, and robot ranging sensor. A voltage reference ladder, comparators, and an encoder are the three basic components of a flash ADC. Due to the analog nature of the comparators and voltage reference ladder, which form the basic analog building blocks of the flash ADC, were redesigned using digital-in-concept circuits.

Different versions of digital-based analog comparators (pseudo comparators) have been proposed to operate across the entire input range. The proposed pseudo comparators have a power dissipation ranging from 75 µW to 196 µW, an offset voltage of less than 4.97 mV, a maximum delay of 2.9 ns and a FOM of 1.2 fJ/conv. To test the functionality, some of the proposed comparators have been implemented on FPGA. Further, fully-digital and synthesizable analog comparators have been proposed. The post layout simulations of the proposed synthesizable voltage comparator show offset, delay and power of 0.72 mV, 0.532 ns and 269.8 µW, respectively and the physical layout area is 728 μm^2.

A novel digital-in-concept voltage reference ladder, consisting of a delay-based network and a time-to-voltage converter has been presented. It operates in the range of 0.46 V to 1.8 V with an LSB of about 20 mV and have a negligible process variation in the delay-based network.

The proposed pseudo comparators have been used to implement 4-bit and 5-bit flash ADCs with FOMs of 0.81 pJ/conv. and 0.55 pJ/conv., respectively. The all-digital 6-bit flash ADC has been implemented using the synthesizable comparator and the digital-in-concept voltage

reference ladder in 180 nm 1.8 V CMOS SCL technology. The physical layout of chip's core occupies an area of 534.53 µm × 301.2 µm and is integrated in a 2 mm × 2 mm die. The proposed all-digital 6-bit flash ADC has a FOM of 1.03 pJ/conv. At a sampling frequency of 400 MHz, the proposed ADC consumes 16.6 mW of power. ENOB, SNDR, SNR, and SFDR for this ADC are correspondingly 5.33, 33.8 dB, 35.2 dB, and 39.73 dB. The values of INL and DNL are +0.7/−0.2 LSB and ±0.5 LSB, respectively. Hence, the proposed all-digital flash ADC is suitable for low power and high speed SoC application with reduced design effort time-to-market.